IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re patent application of

Francesco A. Campisano et al. Confirmation No.: 8459

Serial No.: 10/079,651 Group Art Unit: 2621

Filed: February 20, 2002 Examiner: D. Czekaj

For: LOW LATENCY VIDEO DECODER WITH HIGH-QUALITY, VARIABLE SCALING AND MINIMAL FRAME BUFFER MEMORY

Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

REVISED APPELLANT'S BRIEF UNDER 37 C.F.R. §41.37 AND RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF

This revised brief is in furtherance of the Notice of Appeal, filed in this case on March 27, 2007, following a timely filed Appellant's Brief filed May 29, 2007, and in response to a Notification of Non-Compliant Appeal Brief mailed August 30, 2007. The notification of Non-Compliant Appeal Brief notes that in the description of independent claim 1, no reference is made to the specification. No other point of non-compliance has been indicated. This revised Appellant's Brief supplies such references and summarizes the claimed subject matter of independent claims 1 and 9 and references to the specification and drawings in tabular form but is otherwise substantially identical to the Appellant's Brief file May 29, 2007.

This brief contains these items under the following headings, and in the order set forth below (37 C.F.R. §41.37(c)):

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I. REAL PARTY IN INTEREST

The real party in interest in the appeal is:

☐ the party named in the caption of this brief.

☑ the following party:

International Business Machines Corporation of Armonk, New York

II. RELATED APPEALS AND INTERFERENCES

With respect to other appeals, interferences or judicial proceedings that will directly affect, or be directly affected by, or have a bearing on the Board's decision in this appeal:

☑ there are no related appeals, interferences or judicial proceedings related to, which directly affect or may be directly affected by or have a bearing on the Board's decision in this pending Appeal.

☐ these are as follows:

III. STATUS OF CLAIMS

The status of the claims in this application are:

A. Total number of claims in Application

Claims in the application are:

Claims 1 - 15

B. Status of all the claims:

1. Claims cancelled:

None

2. Claims withdrawn from consideration but not cancelled:

None

3. Claims pending:

Claims 1 - 15

4. Claims allowed:

Claims 6 and 13 (subject to being rewritten in independent form)

5. Claims rejected:

Claims 1 - 5, 7 - 12, 14 and 15

C. Claims on Appeal.

The claims on appeal are:

Claims 1 - 5, 7 - 12, 14 and 15

IV. STATUS OF AMENDMENTS

The status of amendments filed subsequent to the final rejection are as follows:

No proposed amendments have been requested subsequent to the final action in this application. The Advisory Action mailed February 27, 2007, indicates that the Request for Reconsideration filed January 16, 2007, will be entered for purposes of Appeal.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Introduction

The invention as defined in the claims on appeal is directed to methods for solving two interrelated problems in a very complex and demanding environment of a motion video image decoder for decoding compressed data in which user controls over the scaling and positioning of images within a display area is currently being demanded by consumers. Such decoders are usually embodied in so-called set top boxes (STBs) which must be manufactured in large numbers and thus even slight increases in cost to accommodate additional functions can easily become prohibitively expensive.

It should be initially understood that decoding of compressed motion video data may take a variable amount of time and completion within the time available within the fixed time of scanning of a display device (reduced by the vertical blanking interval (vbi)) is not guaranteed. That is, some frames cannot be decoded as rapidly as the display can be scanned, particularly where an interlaced display scan is used for display. However, at the present state of the art, completion within such a time period can generally be accomplished by introducing latency such that decoding can be initiated generally at least one field (0.5 frames for bi-directionally interpolated B frames, 1.5 frames for reference (I) and predicted (P) frames) before readout for display is initiated so that completion of decoding of a frame can generally be completed by the time the last macroblock of the first field (sometimes referred to as a top or odd field) is reached by the display. (Any frames for which decoding is not completed by the time decoded data is needed for display can generally be accommodated without causing corruption of data or introducing distracting visual artifacts in the display by omission of decoding of a frame or, if decoding is completed early, by repeating display of a frame as discussed on pages 3 and 4 of the specification.)

The first problem arises when an image is scaled and positioned such that the bottom of the displayed image is above the bottom of the scanned display area. When an image is displayed over the full screen area, as has previously been deemed satisfactory, the display and the decoding process can be synchronized at the same point in time which is generally chosen to be between fields or frames and, under such circumstances a maximum amount of time is available for the decoding process, as illustrated in Figure 1B and described on pages 15 - 19 of the specification. However, because a frame must be fully decoded and stored in memory before the last macroblock of a first or top field of a frame is reached by the display scan, scaling and positioning of an images such that the bottom of the image is above the bottom of the display scan (producing a bottom border) causes the last macroblock of the image to be needed for display at an earlier point in time, potentially before decoding is complete and, in any case, reducing the amount of time (e.g. interval 36) available to complete such decoding by the amount of time the display requires to scan the bottom border 17, as also illustrated in Figure 1B and discussed in detail on pages 16 - 17 of the specification. The error in computation of the presentation time stamp (PTS) difference reflecting synchronization error also increases with increase of the bottom border scanning time.

This problem could, in theory, be addressed by increasing latency. However, as a practical matter, the increased cost due to provision of sufficient additional memory to accommodate such increased latency would be prohibitive. Further, the problem of increased latency is aggravated by the fact that a top border 15 may be caused by scaling and positioning of the image and additional memory must be provided to store data which is decoded between the time decoding of a frame is initiated and the time the image area is reached since newly decoded data cannot be allowed to overwrite previously decoded data which has not yet been read out for display, or, alternatively and even less feasibly, it would be necessary for the decoding

time to be further reduced by delaying the start of decoding until readout of previously decoded data is begun (see pages 18 - 19 of the specification). Thus, the second, related problem is the cost of additional memory.

Independent claim 1

Independent claim 1 is directed to a solution to the first problem discussed above. Claim 1 recites a step of determining a frame switch point FS in accordance with *completion* of decoding of a previous frame (and is thus variable relative to the scanning synchronization of the display device and the detection of a new frame to be decoded), as shown in Figure 2 and disclosed at page 21 lines 3 - 17 which further detail of an exemplary operation provided in Figure 3 and the discussion thereof on pages 22 - 25 of the specification, and a step of synchronizing the motion video decoder for decoding compressed image data (e.g. initiating decoding of a frame) in accordance with either the (variable) frame switch point (determined in the preceding step based on *completion* of decoding of a previous frame) or the bottom border of the scaled image as disclosed on page 20, lines 3 - 10; which points are illustrated as coincident with each other in Figure 2 (where the bottom border scan time and the recovered decode (DCD) time are depicted as being the same and the FS point is advanced to be coincident with the beginning of the bottom border scanning; both of which are advanced relative to the vertical sync signal V of the display).

In essence, this feature of the invention which supports the meritorious recovery of decoding time resides in *making the frame switch FS point variable* rather than fixed to the vertical sync signal of the display as depicted in Figure 1B by determining the FS point based on the *completion* of decoding of a previous frame which can occur earlier than the beginning of scanning of the bottom border of the display (which is a time limit for completion of decoding) and then synchronizing *decoding* of a frame of image data to either the FS point or the beginning of scanning of the bottom border ~~which is the practical limit of the FS point; *both* of which are~~

significantly advanced from the vertical sync signal V of the display when scaling and positioning of the image causes a bottom border on the display and reduces decoding time. These steps are precisely the steps recited in claim 1.

In summary, basic supporting disclosure for independent claim 1 is found as indicated in the following table. However, it is respectfully submitted that detailed and exemplary supporting disclosure may be found throughout the application including the specification, drawings, abstract and claims and, in view of the complexity of the environment of the invention, the text and illustration noted below should be considered in the context of the entire disclosure, particularly in comparison with Figure 1B and the discussion thereof on pages 15 - 19.

1. A method of operating a motion video decoder for decoding compressed image data, said method including steps of	See Summary of the Invention, page 11
determining a frame switch point in accordance with a signal corresponding to completion of decoding of a previous frame, and	Figure 2, *variable* frame switch, FS, points 42, 44, as described at page 21, lines 3 - 17 (compare with Figure 1B, where the *fixed* FS point 26 is coincident with the initiation 26 of the vertical retrace interval (vbi)
synchronizing said motion video decoder for decoding compressed image data in accordance with one of display of a bottom border of a scaled image and said frame switch point.	Page 20, lines 3 - 10, Figure 2, decoding begun at FS in advance of V, yielding recovered decode (DCD) time (in this case, also coincident with the bottom border.

Independent claim 9

Independent claim 9 is directed to a solution to the second problem alluded to above: avoiding a need for more than minimally increased spill buffer capacity by providing a step of testing the spill buffer capacity and a step of altering the latency and controlling scaling in the decoding path. As discussed at, for example, page 9, line 3+; page 21, lines 18+; page 26, lines 24 +: pages 28 and 29; and, with reference to Figure 4, the paragraph bridging pages 30 - 31, the hardware chip(s) forming the spill buffer will generally have some excess capacity beyond that required to cover the vertical blanking interval for a full screen image to be displayed simply because of the incremental capacities of commercially available chips. As scaling is increased to smaller images and the size (and time to scan) the top and bottom borders is increased, the required capacity of the spill buffer would ordinarily increase. However, if fractional scaling, which reduces the image size by a power of two is performed as an incident of decoding, the amount of decoded data is correspondingly reduced. Therefore, the aspect of the invention to which independent claim 9 is directed provides for testing the spill buffer capacity responsive to a signal (e.g. relative to the current specifications for the top and bottom borders and the vertical blanking interval) which may be sufficient if the top and bottom borders are not a significant fraction of the display area and, if insufficient capacity is found, scaling is controlled (e.g. fractional scaling which reduces data volume) as well as latency since the reduced volume of data can be accommodated in the (e.g. existing) spill buffer even when increased latency is imposed. That is, when the existing spill buffer capacity would be exceeded when the scaling approaches a one-half, one-quarter, one-eighth, etc. size image, the data is reduced by a similar fraction; allowing increased latency to be accommodated by a spill buffer of substantially unchanged capacity through reconfiguration of the frame buffer and spill buffer into respective sections 78, each of which sections 78 can accommodate the reduced data corresponding to a

field within the data capacity for a frame (e.g. two fields) at low latency of image data that is not reduced by fractional scaling. As disclosed, the reduction in data reduces resolution but the resolution of the display remains substantially fully utilized because the size of the image (and number of pixels therein) is correspondingly reduced. Continuous scaling is performed subsequent to the frame and spill buffers and does not affect the required storage capacity since it is performed by interpolation (page 31, line 2) for either expansion or reduction of image size based on unscaled, low latency or fractionally scaled, high latency data and may be viewed as fine scaling while fractional scaling is used for coarse scaling. This claimed combination of testing spill buffer capacity and control of *both* scaling and latency in response to the result also assures that increased latency will be applied only where necessary in view of the existing storage capacity and, conversely, that only a minimal increase, if any beyond the actual capacity of the chip(s) normally employed for an unscaled image, of the spill buffer is required in order to accommodate continuous scaling to any arbitrary degree with complete freedom of control of placement of a scaled image at any arbitrary location on the display.

In summary, basic supporting disclosure for independent claim 9 is found as indicated in the following table. However, it is again respectfully submitted that detailed and exemplary supporting disclosure may be found throughout the application including the specification, drawings, abstract and claims and, in view of the complexity of the environment of the invention, the text and illustration noted below should be considered in the context of the entire disclosure.

9. A method of operating a motion video decoder comprising steps of	See Summary of the Invention, page 11. See also page 9, lines 3+; page 21, lines 18+; page 26, lines 24+ and pages 27 - 31, as illustrated in Figure 4.
testing spill buffer capacity responsive to a signal to produce a test result, and	see page 27, lines 14+, and page 28, lines 5+.
controlling scaling in a decoding path of a decoder and altering decoder latency in response to said test result.	See page 26, lines 34+. and Figure 4 ("Enable Scaling" input to frame buffer and spill buffer).

Dependent claims 2 - 8 and 10 - 15

Claim 2 contains essentially the same recitations as independent claim 9, as discussed above, but depends from claim 1 and thus includes the subject matter thereof, as also discussed above. Dependent claims 3 - 8 and 10 - 15 parallel each other and thus also differ by the subject matter of claim 1. Thus, claims 3 and 10 recite reconfiguration of the frame buffer as shown at 78 of Figure 4 and discussed on pages 30 - 31 to accommodate increased latency. Dependent claims 4 and 11 recite continuous scaling of an image from data fractionally scaled in the decoding path also shown in Figure 4 and discussed on pages 30 - 31. Dependent claims 5 and 12 recite that the continuous scaling is performed by interpolation as noted at page 31, line 2. (Claims 6 and 13 recite latency of reference (I) and interpolated (B) frames and have been indicated at being directed to allowable subject matter.) Dependent claims 7, 8, 14 and 15 recite specific limits of the capacity of the spill buffer (see paragraph bridging pages 21 and 22).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection to be reviewed on Appeal are:

1.) The rejection of claim 1 under 35 U.S.C. §103 as being unpatentable over Simmons et al., and

2.) The rejection of claims 2 - 5, 7 - 12, 14 and 15 under 35 U.S.C. §103 as being unpatentable over Simmons et al. in view of Cheney et al

ARGUMENT VIIA. REJECTIONS UNDER 35 U.S.C. §112, FIRST PARAGRAPH

There are no grounds of rejection under 35 U.S.C. §112, first paragraph.

ARGUMENT VIIB. REJECTIONS UNDER 35 U.S.C. §112, SECOND PARAGRAPH

There are no grounds of rejection under 35 U.S.C. §112, second paragraph.

ARGUMENT VIIC. REJECTIONS UNDER 35 U.S.C. §102

There are no grounds of rejection under 35 U.S.C. §102.

ARGUMENT VIID. REJECTIONS UNDER 35 U.S.C. §103

VIID(1) The rejection of claim 1 as being unpatentable over Simmons et al.

Claim 1 has been rejected under 35 U.S.C. §103 as being unpatentable over Simmons et al. It is respectfully submitted that this ground of rejection is in error since the Examiner has not made a *prima facie* demonstration of obviousness. It is also respectfully submitted that the Examiner has misinterpreted the Simmons et al. reference, evidently through hindsight, and ignored significant explicit recitations of claim 1.

The Examiner admits that Simmons et al. does not teach a frame switch (FS) point but appears to assert that the frame synchronization pattern of Simmons et al. is the same as or an equivalent of the claimed FS point. However, it is respectfully pointed out that the frame synchronization *pattern* of Simmons et al. is much different in many ways from the claimed FS *point*. As pointed out in the Request for reconsideration filed January 16, 2007:

> "First, Simmons et al. describes the FS pattern 66 as a sync signal included with other frame head information 68 in the frame head 62 (Figure 3). Simmons et al. further describes FS pattern 66 as "a data or bit pattern that will ideally only appear in a communication signal when an FS pattern is actually being transmitted and provides for determination of frame timing and other synchronization information by a receiver" (column 5, lines 21 - 25, noted by the Examiner) and also indicates that the remainder of the frame head information (e.g. 68) may "for example, designate a particular decoding process to be used in a receiver" (column 5, lines 25 - 27). As the Examiner observes, when an FS pattern is encountered or detected, a full frame is decoded and upon completion of the decoding, the system of Simmons et al. reverts to a search mode for another FS

pattern, presumably for a next frame (see column 5, lines 38 - 50). The following text then outlines problems associated if a signal pattern which is not an FS pattern is falsely or incorrectly detected as an FS pattern.

"Therefore, it is respectfully submitted to be clear from Simmons et al., in the very passages relied upon by the Examiner, that the FS pattern of Simmons et al. does not answer the explicit claim recitation of "determining a frame switch point in accordance with a signal corresponding to completion of decoding of a previous frame" but, rather, the arrangement of Simmons et al. merely enters a mode to *search for* an FS pattern at the completion of decoding a frame. In short, Simmons et al. refers to a frame synchronization (FS) pattern because that terminology is descriptive of its function while a frame switch point would not be descriptive of its function in Simmons et al. to indicate the *start* of a *frame to be transmitted* and, by the same token, the determination and function of the frame switch point in accordance with the invention which serves to indicate when decoding of a *received or partially received frame can begin* cannot be performed based on a signal that precedes data for a frame and has no temporal relation to a previous frame (or bottom border). This distinction of the invention from Simmons et al. clearly supports the meritorious function of minimizing data latency and spill buffer requirements not available from Simmons et al.

"Further, it is also respectfully submitted to be clear from the passages of Simmons et al. relied upon by the Examiner, as discussed above, that the FS pattern of Simmons et al. does not answer the explicit recitation of "synchronizing said motion video decoder for

decoding compressed image data in accordance with one of display of a bottom border of a scaled image and said frame switch point" even if that recitation could be answered by synchronizing to the frame switch point alone since the frame switch point of the invention is determined upon *completion* of decoding of a frame whereas the FS pattern of Simmons et al. occurs *prior to the frame information* and serves to synchronize the decoding of the frame which *follows* the FS pattern."

In summary, the frame synchronization *pattern* of Simmons et al. is not a point in time but, rather, a *location in a code stream* which indicates the *beginning* of code for a frame and thus cannot be a frame switch (FS) *point which is determined "in accordance with a signal corresponding to completion of decoding of a previous frame"*; explicit language of claim 1 which the Examiner has effectively ignored. Even the term "pattern" is utterly inconsistent with the claim term "point" since a code "pattern" in a data stream necessarily occurs over a period of time and cannot indicate a point in time. Further, the operation of a decoder is only "synchronized" to the frame synchronization pattern of Simmons et al. in the substantially trivial sense that decoding of a frame can begin after a new frame of code is detected which has no particular connection with any timing of a display or completion of decoding of a previous frame. The arrangement of Simmons et al. merely commences a *search* for a frame synchronization pattern in the code after completion of decoding of a previous frame and the frame synchronization pattern may be found substantially later. This mode of operation of Simmons et al. which is sharply contrasted with the invention, as claimed, is also fully admitted by the Examiner on page 2 of the final rejection mailed November 15, 2006, in response to prior remarks.

Additionally, it is respectfully submitted that the Examiner has not properly answered the recitation of synchronization of the decoder "to one of display of a bottom border of a scaled image and said frame switch point". Simmons et al. does

not teach or suggest anything in regard to a scaled image or a bottom border. It logically follows that nothing in Simmons et al. teaches or suggests synchronizing anything to a function that Simmons et al. does not teach or suggest performing and the Examiner has not asserted that it does but has, in fact, admitted that it does not. Likewise, Simmons et al. does not teach synchronization to a frame switch FS point which is determined in the manner recited in the claim and it is clear that the frame synchronization *pattern* of Simmons et al. is clearly not a frame switch FS *point* and cannot properly be considered to be an equivalent thereof for the reasons discussed above. Moreover, in the rejection of a method claim under 35 U.S.C. §103 it is respectfully submitted that the issue is whether the scope and content of the prior art extends so far as to support a conclusion of obviousness of the entirety of the subject matter claimed and thus it is respectfully submitted that, to properly support a conclusion of obviousness, the prior art applied should include evidence of the level of ordinary skill extending to *both* recited alternatives; which evidence the Examiner has also admitted that Simmons et al. does not provide.

Therefore, it is respectfully submitted that the Examiner has not made a *prima facie* demonstration of obviousness through a clear and convincing line of reasoning, but, rather, has admitted both that the frame synchronization *pattern* of Simmons et al. does not directly answer the recitation of frame switch *point* and admitted differences therebetween which precludes a finding of equivalency. The frame synchronization pattern is completely different in nature and function from the claimed frame switch point such that it is unsuitable for the function explicitly recited in the claim and is derived/detected in a manner completely different from that explicitly claimed (which recitation has been effectively ignored) and such that any possible parallel between the two can be reached only through hindsight. Therefore, it is respectfully submitted that this ground of rejection is clearly in error and untenable.

VIID(2) Rejection of Claims 2 - 5, 7 - 12 14 and 15 under 35 U.S.C. §103 As Being Unpatentable Over Simmons et al. in view of Cheney et al.

Claims 2 - 5, 7 - 12, 14 and 15 have been rejected under 35 U.S.C. §103 as being unpatentable over Simmons et al. in view of Cheney et al. It is respectfully submitted that this ground of rejection is also in error and untenable since the Examiner has clearly ignored explicit recitations of the claims; which failure necessarily precludes a *prima facie* demonstration of obviousness from being made.

VIID(2)(a) Rejection of Independent Claim 9

It is initially to be noted that the Examiner's statement of the rejection makes reference to Sazzad. It is believed that this mention is an incident of a previously applied ground of rejection which has been overcome.

In regard to independent claim 9 (and dependent claim 2), the Examiner asserts that Cheney et al. teaches use of a spill buffer and controlling decoder latency. However, Cheney et al. is not seen to teach or suggest (particularly in the passages of column 14 of Cheney et al. relied upon by the Examiner) any scaling or positioning of the image on the display and thus cannot provide evidence of the level of ordinary skill in the art extending even to the recognition of the problem of the increase of required spill buffer capacity to cover top and bottom border display scan times much less the solution thereto as claimed. There is no indication in Cheney et al. that the spill buffer is used in any manner other than what is indicated to be conventional for full frame image display where the spill buffer need only cover the vertical blanking interval. Further, the passages relied on by the Examiner do not discuss any change in latency but only delay of decoding a subsequent frame if decoding of a given frame is completed early. (By the same token, Cheney et al. teaches away from synchronization of the decoder to the frame switch point as discussed above in connection with claim 1 and thus does not mitigate the deficiencies of Simmons et al. discussed above.)

More specifically, there is no teaching or suggestion in Cheney et al. of any testing of the spill buffer but only determining if an address exceeds the capacity of another buffer distinct from the spill buffer to which the spill buffer may be assigned or appended if necessary to avoid overwriting/collision of data. as pointed out above, there is no change in latency (e.g. a change of multiples of a field time) performed in response to any test but only a delay provided when decoding is completed early. More importantly, there is no teaching or suggestion of scaling in Cheney et al. much less control of scaling (and even less scaling in a decode path, as explicitly recited) in response to the result of a test of the spill buffer (which Cheney et al. does not perform) as to which the Examiner's statement of the rejection is completely silent. The Examiner has not asserted anything in Cheney et al. which corresponds to a *combination* of functions (e.g. control of scaling *and* change of latency) which are explicitly recited as being performed based on a result of a test of the *spill buffer* (which Cheney et al. also fails to teach or suggest). Therefore, it is respectfully submitted that the Examiner has not only failed to make a *prima facie* demonstration of obviousness of claim 9 based on Simmons et al. and Cheney et al. but has failed to address salient explicit recitations of the claim but has clearly misconstrued the teachings of Cheney et al. in a manner which, it is respectfully submitted, can only be reached through impermissible hindsight while not demonstrating that the teachings of Simmons et al. and Cheney et al. are properly combined or even properly combinable since it appears that modification of Simmons in accordance with Cheney et al. would preclude operation of Simmons et al. in the manner intended (see In re Gordon, 221 USPQ 1125 (Fed.Circ, 1984)) for the reasons discussed above. In point of fact, Cheney et al. does not contain teachings of suggestions which answer *any* recitations of claim 9. Accordingly, it is respectfully submitted that this ground of rejection is also clearly in error and untenable.

VIID(2)(b) Rejection of Dependent Claim 2

As pointed out above, claim 2 contains the same recitations as independent claim 9 but differs by dependency from independent claim 1. Therefore, it is respectfully submitted that the rejection of claim 2 is clearly improper and untenable for the reasons discussed above in regard to claim 9. Additionally, it is respectfully submitted that Cheney et al. does not mitigate the deficiencies of Simmons et al. in regard to the subject matter of claim 1 and is not properly combined or combinable therewith. Accordingly, it is respectfully submitted that this ground of rejection is clearly in error and untenable in regard to claim 2.

VIID(2)(c) Rejection of Claims 3 and 10

Initially, it is respectfully submitted that while claims 3 and 10 contain substantially the same recitations, they do not stand of fall together since claim 3 differs from claim 10 by the inclusion of the subject matter of claim 1.

It is respectfully submitted that Cheney et al. does not teach or suggest reconfiguring the frame buffer and particularly not for the purpose of accommodating an increased latency (which increased latency Cheney et al. does not teach or suggest, as pointed out above. Cheney merely "steers the address to a point in the Spill Buffer" (column 14, lines 32 - 33) and does not, in fact, perform any reconfiguration whatsoever of the frame buffer. Therefore, it is respectfully submitted that the rejection of claims 3 and 10 is also clearly in error and untenable.

VIID(2)(d) Rejection of Claims 4 and 11

Again, it is respectfully submitted that while claims 4 and 11 contain substantially the same recitations, they do not stand of fall together since claim 4 differs from claim 11 by the inclusion of the subject matter of claim 1.

As pointed out above, neither Cheney et al. nor Simmons et al. teaches or suggests any scaling function or how such a function could be accomplished much less any "continuous scaling from motion video data scaled in said decoding path".

The Examiner, in the statement of the rejection does not address this explicitly recited feature of the invention at all and the reference to a passage of column 9 and Figure 5 of Cheney et al. is only asserted (incorrectly) in regard to the subject matter of claims 5 and 12, as will be discussed below. Therefore, it is respectfully submitted that this ground of rejection is clearly in error and untenable in regard to each of claims 4 and 11.

VIID(2)(e) Rejection of Claims 5 and 12

Again, it is respectfully submitted that while claims 5 and 12 contain substantially the same recitations, they do not stand of fall together since claim 5 differs from claim 12 by the inclusion of the subject matter of claim 1.

In regard to this ground of rejection, the Examiner asserts that Figure 5 and column 9, lines 66 - 67 teach scaling of motion video data by interpolation. This assertion is clearly erroneous. Figure 5 does not illustrate any structure having anything whatsoever to do with scaling and column 9 (and following text) is clearly directed to "interpolation to form predicted image blocks" (column 10, line 1 - e.g. the decoding of predicted or "P" images). Therefore, it is respectfully submitted that this ground of rejection is clearly in error and untenable as applied to claims 5 and 12.

VIID(2)(f) Rejection of Claims 7 - 8 and 14 - 15

Again, it is respectfully submitted that while claims 7 - 8 and 14 - 15 contain substantially the same recitations, they do not stand of fall together since claims 7 - 8 differ from claims 14 - 15 by the inclusion of the subject matter of claim 1.

These claims are directed to the capacity of the spill buffer and while Cheney et al. discloses a capacity of the spill buffer to be set at 256 lines rather than the conventional 64 lines, both of which are presumably less than 0.5 fields (claims 7 and 14) or one field (claims 8 and 15), that capacity is thus fixed and, as pointed out above, need not be tested as recited in claims 2 and 9 (e.g. relative to scaling and borders) which Simmons et al and Cheney et al. do not teach or suggest. These

claims recite limits to which the spill buffer capacity may be held *while accommodating borders and scaling* by virtue of the method steps recited in claims 2 and 9, as discussed above. Therefore, Neither Simmons et al. nor Cheney et al., taken singly or together, provides any evidence that the level of ordinary skill in the art extended to such limitation of spill buffer capacity being achieved for other than full screen images. Accordingly, it is respectfully submitted that this ground of rejection is in error and untenable in regard to claims 7, 8, 14 and 15.

ARGUMENT VIIE. REJECTION OTHER THAN 35 U.S.C. §§102, 103 AND 112

There are no grounds of rejection other than under 35 U.S.C. §§102, 103 or 112.

VIII. CLAIMS APPENDIX

The text of the claims involved in the appeal are:

1. A method of operating a motion video decoder for decoding compressed image data, said method including steps of

determining a frame switch point in accordance with a signal corresponding to completion of decoding of a previous frame, and

synchronizing said motion video decoder for decoding compressed image data in accordance with one of display of a bottom border of a scaled image and said frame switch point.

2. A method as recited in claim 1, comprising further steps of

testing spill buffer capacity responsive to said signal to produce a test result, and

controlling scaling in a decoding path of said decoder and altering decoder latency in response to said test result.

3. A method as recited in claim 2, including the further step of

reconfiguring a frame buffer to accommodate a increased latency of motion video data scaled in said decoding path.

4. A method as recited in claim 3, including the further step of

continuously scaling a motion video image from said motion video data scaled in said decoding path.

5. A method as recited in claim 4, wherein said continuously scaling step is performed by interpolation.

6. A method as recited in claim 1, wherein decoder to display latency of reference motion video images is 1.5 frames and latency of interpolated motion video images is 0.5 frames.

7. A method as recited in claim 2, wherein said spill buffer has a capacity equal to or less than 0.5 fields.

8. A method as recited in claim 2, wherein said spill buffer has a capacity equal to or less than one field.

9. A method of operating a motion video decoder comprising steps of

testing spill buffer capacity responsive to a signal to produce a test result, and

controlling scaling in a decoding path of a decoder and altering decoder latency in response to said test result.

10. A method as recited in claim 9, including the further step of

reconfiguring a frame buffer to accommodate a increased latency of motion video data scaled in said decoding path.

11. A method as recited in claim 10, including the further step of

continuously scaling a motion video image from said motion video data scaled in said decoding path.

12. A method as recited in claim 11, wherein said continuously scaling step is performed by interpolation.

13. A method as recited in claim 9, wherein decoder to display latency of reference motion video images is 1.5 frames and latency of interpolated motion video images is 0.5 frames when said testing step indicates spill buffer capacity is sufficient for selected scaling of said motion video.

14. A method as recited in claim 9, wherein said spill buffer has a capacity equal to or less than 0.5 fields.

15. A method as recited in claim 10, wherein said spill buffer has a capacity equal to or less than one field.

IX. Evidence Appendix

No additional evidence is relied upon in this Appeal.

X. RELATED PROCEEDINGS APPENDIX

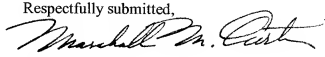
There are no other proceedings relating to this Appeal.

Conclusion

For the reasons set forth above, it is respectfully submitted that the grounds of rejection which have been asserted by the Examiner are clearly in error. The Examiner has effectively ignored explicit significant claim recitations in regard to every claim rejected. Further, the Examiner has misconstrued the each of the references applied against the claims, evidently through impermissible hindsight, to the point of admitted differences in regard to Simmons et al. precluding the identity or equivalence of the frame synchronization *pattern* disclosed therein (which the Examiner has further confused by referring to it as an "FS pattern", seemingly to gloss over the numerous points of distinction from the FS point claimed) to the frame switch *point* claimed and, in regard to Cheney, et al. such that application of Cheney to each recitation of the claims is demonstrably in error under 35 U.S.C. §103 in regard to the asserted scope and content of the prior art. Further, the scope and content prior art applied does not even extend to recognition of the environment (e.g. providing image scaling and display of borders from compressed data which is decoded in real time to provide the illusion of motion) in which the problems which are solved by the invention would arise. Thus, the scope and content of the prior art applied simply does not extend so far as to support a conclusion of obviousness in regard to any claim rejected under either ground of rejection asserted by the Examiner in accordance with the objective analysis required by Graham v. John Deere, 383 U.S. 1 (1966) under 35 U.S.C. §103. The differences between the claimed subject matter and the scope and content of the prior art are numerous and highly distinctive and the Examiner merely applies hindsight upon hindsight to seek some arguable manner in which to assert obviousness and has failed to do so by any compelling line of reasoning while ignoring numerous explicit recitations of the claims. Accordingly, the Examiner has clearly failed to make a *prima facie* demonstration of either ground of rejection which has been asserted and reversal of the Examiner in regard to the

asserted grounds of rejection is respectfully submitted to be clearly in order and such action is respectfully requested.

Respectfully submitted,



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